REMARKS

Pending claims

Claims 1-9 have been cancelled without prejudice. Claims 10-20 were previously cancelled without prejudice. Applicant reserves the right to prosecute the cancelled claims in one or more separately filed continuation patent applications. Claim 21, an independent claim, has been introduced.

Claim rejections under 35 USC 103

Claims 1-5 have been rejected under 35 USC 103(a) as being anticipated by Williams (2003/0110356) in view of Palanca (6,223,258). Claims 6-9 have been rejected under 35 USC 103(a) as being unpatentable over Williams in view of Palanca, and further in view of Chryson (6,549,930). As noted above, claims 1-9 have been cancelled without prejudice, rendering these rejections moot. However, Applicant has submitted a new independent claim, claim 21, that Applicant respectfully submits is not rendered unpatentable over Williams in view of Palanca and Chryson.

Applicant notes that the terminology "first memory line" and "second memory line" in claim 21 has been "switched" as compared to the previously presented claims 1-9. That is, in claim 21, the first memory line is that which is temporarily stored within a buffer and that is not currently cached in a cache, and the second memory line is the memory line that is to be evicted. By comparison, in claims 1-9, the first memory line was that which was to be evicted, and the second memory line was that which was temporarily stored in the buffer.

Claim 21 basically captures the process described on page 10, paragraphs 40-41, and on pages 5-6, paragraphs 25-28, of the patent application as filed. Thus, a first transaction is input into a multiple-stage pipeline to convert the first transaction into a set of concurrently performable actions to process the first transaction. After the first transaction has been input into

the multiple-stage pipeline, and while the first transaction is being converted to the set of concurrently performable actions using the multiple-stage pipeline, the following is performed.

Particularly, in response to determining, within the multiple-stage pipe, that the first transaction requires a first memory line that is not currently cached in a cache, the following is performed. The first memory line is temporarily stored within a data transfer buffer to which the multiple-stage pipeline is directly communicatively connected. In response to determining, within the multiple-stage pipeline, that a second memory line current cached in the cache has to be evicted to make room for the first memory line (where the first memory line is different than the second memory line), the method stores eviction data (regarding the second memory line currently cached in the cache) within the data transfer buffer, and spawns an eviction transaction regarding the second memory line, where the eviction transaction is different than the first transaction.

Now, after the first transaction has been converted to the set of concurrently performable actions using the multiple-stage pipeline, the method performs the following. The method performs the set of concurrently performable actions utilizing the first memory line as temporarily stored within the data transfer buffer. Furthermore, the method places the second memory line in an eviction queue, which is different than the data transfer buffer. The method finally, after the eviction transaction has been spawned, inputs the eviction transaction into the multiple-stage pipeline to process eviction of the second memory line.

Applicant has reviewed Williams in view of Palanca and Chryson in detail, and respectfully submits that these prior art references in combination do not rise to the level of rendering the newly introduced claim 21 obvious and unpatentable. In particular, the method performs various parts or steps in a specific order, and responsive to certain events occurring: (1) some parts or steps are performed *after* inputting the first transaction into the multiple-stage pipeline; (2) some parts or steps are (also) performed *in response to* determining that the first transaction requires a first memory line that is not currently cached in the cache; (3) some parts or steps are (also) performed *in response to* determining that a second memory line currently

cached has to be evicted to make room for the first memory line; (4) some parts or steps are performed *after* the first transaction has been converted to the concurrently performable actions; and, (5) some parts or steps are performed *after* the eviction transaction regarding the second memory line has been spawned. Williams in view of Palanca and Chryson does not rise to the level of suggesting such a specific method in which various parts or steps are performed in a particular order and responsive to certain events occurring. That is, even if "bits and pieces" of the claimed invention are variously suggested by the prior art in combination, what is not suggested by the prior art in combination is the specific ordering of these "bits and pieces" as in the claimed invention.

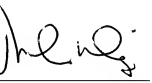
Furthermore, the method performs various parts or steps *within* the multiple stage pipeline. For example, determining that the first transaction requires a first memory line that is not currently cached in a cache is performed within the multiple-stage pipeline, and determining that a second memory line currently cached has to be evicted to make room for the first memory line is also performed within the multiple-stage pipeline. While Chryson shows a multiple-stage pipeline, there is no suggestion within the prior art that this functionality of the invention is performed within the multiple-stage pipeline of Chryson, for instance.

Finally, various functionality and other limitations are recited in the method that are not suggested by any of the prior art references, such that the prior art references in combination cannot be considered in total as suggesting the claimed invention. For example, the claimed invention is limited to performing the set of concurrently performable actions utilizing the first memory line *as temporarily stored within the data transfer buffer*. None of the prior art, either alone or in combination, suggests performing these actions utilizing the first memory line as temporarily stored within the data transfer buffer. For example, the prior art in combination is silent as to whether the set of concurrently performable actions is performed utilizing the first memory line *as may have already been cached*, which the invention does not cover, or *as is temporarily stored within the data transfer buffer*, which the invention does cover. As another example, in the claimed invention, various functionality is performed within the multiple-stage

pipeline in relation to a data transfer buffer that is directly communicatively connected to the multiple-stage pipeline. The prior art in combination does not suggest such functionality being performed within such a pipeline in relation to a data transfer buffer that is directly communicatively connected to the pipeline.

For any and all of these reasons, therefore, Applicant respectfully submits that the claimed invention is *prima facie* nonobvious and patentable over the cited prior art in combination, and requests the allowance of claim 21.

Respectfully Submitted,



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